REMARKS

I. Introduction

By the present Amendment, claims 1, 2, and 9 have been amended, and claim 3 canceled. Claims 10-12 are newly presented for consideration. Claims 4-7 are withdrawn from consideration. Accordingly, claims 1, 2, and 8-12 are now pending in the application. Claims 1, 10, and 11 are independent.

II. Office Action Summary

In the Office Action of April 7, 2005, claims 2 and 3 were objected to because of several informalities. Claim 9 was rejected under 35 USC §112, second paragraph. Claims 1-3 and 8-9 were rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,949,502 issued to Matsunaga et al. ("Matsunaga") in view of U.S. Patent No. 5,914,763 issued to Fujii et al. ("Fujii"). These rejections are respectfully traversed.

III. Claim Objections

Claims 2 and 3 were objected to because of various informalities. The cancellation of claim 3 renders this rejection moot with respect to that claim. Regarding claim 2, the Office Action indicates that the recitation "and the first gate connecting lines are positioned at a higher level than the second gate connecting lines" is unclear. Specifically, the Office Action indicates that it is not known as to what the higher level is relative to with respect to other elements in the claim.

By the present Amendment, Applicants have amended claim 2 to specify that the first gate connecting electrodes are positioned at a higher level than the second gate connecting electrodes within the first substrate. Accordingly, the location of the

first gate connecting lines relative to the second gate connecting lines as well as the other elements of the claim should be clear.

Applicants respectfully request withdrawal of this objection.

IV. Rejections Under 35 USC §112, second paragraph

Claim 9 was rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. With respect to this rejection, the Office Action indicates that claim 9 recites "one of the first gate connecting lines is disposed between two adjacent ones of the second gate connection lines when viewed in plan view." The Office Action further states that the location of the first gate connecting line is unclear because there cannot be two second gate connection lines, and further that it is not known to what "two adjacent ones" refers.

By the present Amendment, Applicants have amended claim 9 to properly indicate that when the liquid crystal display device is examined from a plan view, the first gate connecting lines are positioned between two second gate connecting lines which are adjacent to one another. This feature can be seen through examination of, for example, Fig. 5.

It is therefore respectfully submitted that, as amended, claim 9 satisfies the requirements of 35 USC §112, second paragraph. Accordingly, withdrawal of this rejection is respectfully requested.

V. Rejections Under 35 USC §103

Claims 1-3 and 8-9 were rejected under 35 USC §103(a) as being unpatentable over Matsunaga in view of Fujii. Regarding this rejection, the Office Action alleges that Matsunaga discloses and teaches that a conventional liquid crystal display device has two transparent insulating substrates that enclose a layer

of liquid crystal material. Matsunaga is further alleged as disclosing additional features of claim 1 such as gate lines that include first gate lines and second gate lines, first gate connecting lines and second gate connecting lines disposed in the peripheral area, respective first gate connecting lines electrically connecting the first gate lines to a liquid crystal driving circuit, and respective second gate lines electrically connecting the second gate lines to the liquid crystal driving circuit. The Office Action admits that Matsunaga does not appear to specify that the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate. Fujii is relied upon as teaching this particular feature. The Office Action indicates that Fujii teaches connection electrodes and lead out wirings arranged on sides of two substrates in a liquid crystal display device. Thereafter, the two substrates each bearing the connection electrodes and leadout wirings are stacked together at which point the connection electrodes and leadout wirings are mutually stacked with respect to each other. Reference is directed to column 14, lines 12-46 of Fujii. As amended, independent claim 1 defines a liquid crystal display device that comprises:

> a first substrate, a second substrate, a liquid crystal layer between the first substrate and the second substrate, wherein
> the first substrate has a pixel area, a peripheral area, gate lines, drain lines, first gate connecting lines, second gate connecting lines, a first insulating film, and a second insulating film,
> the pixel area includes pixel electrodes, the gate lines and the drain lines,
> the peripheral area surrounds the pixel area,
> the gate lines include first gate lines and second gate lines,
> first gate connecting lines and second gate connecting lines are disposed in the peripheral area,
> the respective first gate connecting lines electrically connect the first gate lines to a liquid crystal driving circuit,
> the respective second gate connecting lines electrically connect the second gate lines to the liquid crystal driving circuit,
> the first insulating film insulates the first gate connecting lines from the second gate connecting lines,

the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate,

the second insulating film is formed as a higher layer than the first gate connecting lines within the first substrate, and

the second insulating film is formed in the pixel area and the peripheral area.

According to independent claim 1, the gate lines include first gate lines and second gate lines which are disposed in the peripheral area of the first substrate. Respective first gate connecting lines electrically connect the first gate lines to a liquid crystal driving circuit, while respective second gate connecting lines electrically connect the second gate lines to the liquid crystal driving circuit. The first insulating film is used to insulate the first gate connecting lines from the second gate connecting lines. According to independent claim 1, the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate. Additionally, the second insulating film is formed at a higher layer than the first gate connecting lines and the second gate connecting lines within the first substrate. The second insulating film is also formed in the pixel area and the peripheral area.

The Office Action alleges that Fujii discloses a liquid crystal display device having first gate connecting lines and second gate connecting lines stacked in a thickness direction of the first substrate as set forth in independent claim 1. This is not the case, however. Fujii discloses a liquid crystal display device having the electrode wirings on the upper and lower electrode substrates. See column 13, lines 12-14. The two electrode substrates, are stacked together at a point where the connection electrodes and leadout wirings are mutually stacked with respect to each other. See column 14, lines 39-43. Accordingly, the liquid crystal display device of Fujii provides an upper substrate that contains electrode wirings as well as a lower substrate that contains electrode wirings.

This appears contrary to the invention defined by independent claim 1 wherein the first gate connecting lines and the second gate connecting lines are stacked within the first substrate. Rather, it is the two substrates of Fujii that are stacked and not the gate connecting lines. More particularly, Fujii fails to either disclose or suggest a liquid crystal display device wherein "the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate."

It is therefore respectfully submitted that independent claim 1 is allowable over the art of record.

Applicants have recently become aware of Japanese Patent Publication No. JP 2001-274551 to Watanabe which discloses a multi-layer printed circuit board that can be used with a liquid crystal display device. A copy of Watanabe (including English translation) is being submitted with an Information Disclosure Statement together with the present Amendment. Watanabe provides a multi-layer printed circuit board wherein a plurality of wiring layers are arranged along the same plane and stacked in the thickness direction of the layer. In addition, the layers include a plurality of conductors therein. However, Watanabe does not provide an insulating film that is formed in the pixel area and the peripheral area. Further, Watanabe does not appear to disclose a second insulating film being formed at a higher level than the first gate connecting lines and the second gate connecting lines within the first substrate. Specifically, Watanabe fails to either disclose or suggest:

> the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate,
> the second insulating film is formed as a higher layer than the first gate connecting lines within the first substrate, and
> the second insulating film is formed in the pixel area and the peripheral area.

Applicants therefore respectfully submit that independent claim 1 is allowable over Watanabe.

Claims 2, 8, and 9 depend from independent claim 1, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 1. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

Independent claim 10 is newly presented and defines a liquid crystal display device that comprises, in part:

> the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate, and
> one of the first gate connecting lines is disposed between the two second gate connecting lines which are adjacent one another when viewed in plan view.

At least one feature of independent claim 10 provides for the first gate connecting lines to be disposed between two second gate connecting lines which are adjacent to one another when viewed in a plan view. This particular feature is also illustrated in Fig. 5 of the instant application. As previously discussed with respect to independent claim 1, Fujii and Matsunaga fail to disclose first gate connecting lines and second gate connecting lines that are stacked in a thickness direction of a first substrate. However, none of the art of record either discloses or suggests a liquid crystal display device wherein:

> "one of the first gate connecting lines is disposed between the two second gate connecting lines which are adjacent one another when viewed in plan view."

It is therefore respectfully submitted that independent claim 10 is allowable over the art of record.

Independent claim 11 defines a liquid crystal display device that comprises:

a first substrate, a second substrate, a third substrate, a fourth substrate, a first liquid crystal layer between the first substrate and the second substrate, and a second liquid crystal layer between the third substrate and the fourth substrate, wherein

the first substrate has a first pixel area, a first peripheral area, first gate connecting lines, and second gate connecting lines,

the third substrate has a second pixel area and a second peripheral area,

the first pixel area has first pixel electrodes, first gate lines, and first drain lines,

the first peripheral area surrounds the first pixel area,

the second pixel area has second pixel electrodes, second gate lines, and second drain lines,

the second peripheral area surrounds the second pixel area,

the first gate connecting lines and the second gate connecting lines are disposed in the first peripheral area,

the respective first gate connecting lines electrically connect the first gate lines to a liquid crystal driving circuit,

the respective second gate connecting lines electrically connect the second gate to the liquid crystal driving circuit, and

the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate.

According to independent claim 11, the liquid crystal display device comprises a first substrate, a second substrate, a third substrate, a fourth substrate, a first liquid crystal layer between the first substrate and the second substrate, and a second liquid crystal layer between the third substrate and the fourth substrate. The first substrate has a first pixel area, a first peripheral area, first gate connecting lines, and second gate connecting lines. The third substrate has a second pixel area and a second peripheral area. Additionally, the first gate connecting and the second gate connecting lines are stacked in a thickness direction of the first substrate. This particular combination of features and elements does not appear to be disclosed by the art of record taken individually or in combination.

It is therefore respectfully submitted that independent claim 11 is allowable over the art of record.

Claim 12 depends from claim 11, and is therefore believed allowable for at least the reasons set forth above with respect to independent claim 11. In addition,

claim 12 introduces novel elements that independently render it patentable over the art of record.

VI. Rejections Under 35 USC §103

For the reasons stated above, it is respectfully submitted that all of the pending claims are now in condition for allowance. Therefore, a Notice of Allowance is believed in order, and courteously solicited.

If the Examiner believes that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

Docket No. 501.42822X00
Serial No. 10/618,748
Office Action date April 7, 2005

AUTHORIZATION

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 501.42822X00).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP.

Leonid D. Thenor
Registration No. 39,397

LDT/vvr
1300 N. Seventeenth Street
Suite 1800
Arlington, Virginia 22209
Tel: 703-312-6600
Fax: 703-312-6666

Dated: October 7, 2005